ASSIGNMENT 1

Submission Date: 22/7/2017

Chapter: 1

1) Explain major steps involved in digital design using CAD tools.
2) Give difference between software language and Hardware language.
3) Write a short note on FPGA and also list out the difference between CPLD and FPGA.
4) List the 9 values of std_logic
5) List the major capabilities of VHDL along with the features.
6) Explain data types used in VHDL.

ASSIGNMENT 2

Submission Date: 12/8/2017

Chapter 2, 3

1) Explain different abstraction level of Digital design. Also give difference between top-bottom and bottom-top methodologies for digital design.
2) Explain configuration and package declaration statements using necessary examples.
3) Explain Package and library with suitable example.
4) Write brief note on VHDL data types.
5) Explain various predefined operators in VHDL with their precedence.

ASSIGNMENT 3

Submission Date: 1/9/2017

Chapter 4 , 5

1) What is difference between signal and variable with example?
2) What do you mean by Delta-delay? Also explain Inertial Delay model and Transport Delay model.
3) Write a HDL code (VHDL/verilog) 4 – Bit full – adder using behavioral modeling.
4) Give difference between Moore FSM and Mealy FSM. Draw Moore FSM for BCD counter. Also write HDL code (VHDL/verilog) code for BCD Counter using Moore FSM model.
5) Draw a state diagram for moore type finite state machine which generates output '1' when receives input string sequence '111' on three subsequent clock cycles. Include Reset signal which bring FSM to initial state when it goes to high. Write HDL code (VHDL/verilog) code for this FSM using process statement.
6) Explain different wait statements. What will be the effect of including 'wait for 0 ns' statement within the middle of process statement which has signal assignments statements before and after this wait statement? Explain with appropriate example.
7) Explain Assertion statement. Explain its usefulness in writing testbench
8) Write a brief note on generics and configuration.
9) Explain briefly variable assignment and signal assignment statement with example.
10) Explain modeling of MOOREY FSM with state diagram and code.
11) Explain modeling of Mealy FSM with state diagram and code.
12) What are purposes of Block statement?
13) Differentiate between concurrent and sequential signal assignment statement.
14) Differentiate between exit and next statements
15) Discuss types of FSM (finite state machine) with appropriate example.

ASSIGNMENT 4

Submission Date: 26/9/2017

Chapter 6,7

1) What is FPGA? Draw its basic structure and give its applications
2) Using structural modeling implement 9bit parity generator using HDL code (VHDL/verilog).
3) Write a HDL code (VHDL/verilog) for ALU for different operations.
4) Explain CPLD Architecture in brief.
5) Draw and explain digital design flow for FPGA.
6) Give the generic architecture for PLA, PAL
7) Explain Programmable Logic devices. Also give comparison between PAL, PLA, CPLD and FPGA

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