Bhagwan Mahavir College of Engineering & Technology
Academic Year: 2017-2018
6th Sem EC
Subject: VLSI Technology & Design (2161101)

Assignment -1 **Submission date: 23-01-2018**

Chapter 1, 2 (As per GTU Syllabus)

1. Explain VLSI Design Flow.
2. Explain Design hierarchy, regularity, modularity and locality.
3. What are three main domains in Y chart of VLSI Design flow?
4. Why nMOS is better then pMOS transistor?
5. What is the fundamental difference between MOSFET and BJT?
6. Describe fabrication process of MOSFET.
7. Write short note on Layout Design rules.
8. What are the advantages of ion implantation over diffusion?
9. What is the difference between positive photoresist and negative photoresist? Which is commonly used in the manufacturing of high density integrated circuits?

Mrs. Hiral Patel
HOD, EC & Elx.

Assignment -2 **Submission date: 13-02-2018**

Chapter 3, 4 (As per GTU Syllabus)

1. Derive the expression of threshold voltage of an n-channel MOSFET.
2. Explain the following:
   (i) Channel length modulation
   (ii) Substrate bias effect

3. Explain the energy band diagram of MOS structure at surface inversion and derive the expression for the maximum possible depth of the depletion region.

4. Calculate the drain current of nMOS if source terminal is connected to ground and

   Vg = 1.8V Vd = 1 V Vth = 1V

   μ_n= 400 cm^2/VS Cox = 800uF $(W/L)_n$=1.5

5. Explain the concept of MOSFET as a switch.
6. Write short note on resistive load Inverter. Derive the expression of V_{OH}, V_{OL}, V_{IL}, V_{IH} of a resistive load inverter.
7. Draw a typical test circuit arrangement for the measurement of K_n, V_{TO} , CLM parameter (λ) and γ of an n-channel MOSFET. Explain how the parameters are measured.

8. For a CMOS inverter with following specification compute V_{IL}, V_{IH} and find out inverter is symmetric or not?

   VDD = 1.8V Vtn= 0.5 V Vtp= -0.5 V

   μ_n= 580 cm2/VS μ_p= 290 cm/VS $(W/L)_p = 2(W/L)n$

9. Draw CMOS Inverter circuit. Obtain expressions for V_{IL} and V_{th}.

10. Calculate the threshold voltage V_{TO} under zero bias at room temperature (T=300°K), for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 10^{20}$ cm^{-3}, t_{ox} = 500°A, and oxide interface fixed charge density $N_{OX} = 2 \times 10^{10}$ cm^{-3}. Take $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm, $\varepsilon_{si} = 11.7 \times \varepsilon_0$ F/cm, $\varepsilon_{ox} = 3.97 \times \varepsilon_0$ F/cm.

11. What is short channel effect? Derive expression for the change in threshold voltage due to short channel effect.

12. Comparison of Full-scaling and Constant voltage scaling.

Mrs. Hiral Patel
HOD, EC & Elx.

Assignment -3 **Submission date: 28-02-2018**

Chapter 5,6 (As per GTU Syllabus)

1. Explain Elmore delay calculation method for complex RC network. Derive the formula for Elmore delay.
2. Explain two input depletion load NOR gate and derive the necessary equations for the same.
3. Draw input and output waveform during high to low transition of output for a CMOS inverter and derive expression for τ_{PHL}.
4. Draw and discuss three stage ring oscillator circuit.
5. Derive equivalent resistance of the CMOS transmission gate (pass gate), and plot it as a function of the output voltage.
6. Implement the following Boolean function using CMOS F=[(C+D+E)(B+A)]' find a equivalent CMOS inverter circuit simultaneous switching of all inputs. Assume $(W/L)_p$=15 for all pmos transistor and $(W/L)_n$= 10 for all nmos transistor.
7. Explain the functioning of CMOS transmission gate. Draw six-transistor CMOS -TG implementation of the XOR function.

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Assignment -4 **Submission date: 20-03-2018**

Chapter 7,8 (As per GTU Syllabus)

1. For XOR function, draw following implementations.
   a. Full CMOS gate
   b. Pseudo-nMOS gate
   c. CMOS transmission gate(TG)
2. Explain the principle of dynamic CMOS logic (Precharge-Evaluate logic). Discuss its advantages and disadvantage.
3. Draw CMOS implementation of D latch with two inverters and two CMOS TG gates. Explain its working.
4. What is the need of voltage bootstrapping? Draw dynamic boot-strapping arrangement and explain it.
5. Draw the circuit diagram of domino CMOS logic gate and discuss it in detail.
6. Draw the circuit diagram of a CMOS edge-triggered D-latch and explain.
7. Explain the basic principle of pass transistor circuit. Explain logic '1' transfer and logic '0' transfer.

Mrs. Hiral Patel
HOD, EC & Elx.

Assignment -5 **Submission date: 10-04-2018**

Chapter 9,10 (As per GTU Syllabus)

1. Discuss remedies of CMOS Latch-Up.
2. Ad hoc testable design techniques.
3. Write a short note on Built In Self Test(BIST).
4. Short Note: FPGA
5. Comparison of FPGA and CPLD.
6. Controllability and observability

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